Claims:

What is claimed is:

1. A method for yield improvement of VLSI integrated circuits by self-consistent minimization of process and design interactions, said method comprising the steps of:

a) inputting a design data set that define a pre-selected chip design including layout data and circuit design data which define electrical functionality of said IC design

b) performing circuit sensitivity analysis to determine acceptable range of circuit element characteristics based on the predefined nominal circuit performance specifications

c) performing IC manufacturing process characterization to extract nominal device models and quantify device sensitivities to geometry distortions

d) using data gathered in step b) and c) to determine maximum layout correction unit and acceptable range of geometry distortion for all devices

e) identifying devices on the layout

f) further identifying electrically relevant edge sections and subdividing those into segments on which subsequent correction is to be performed. Segment size is calculated in step d)

g) performing simulation of lithographic process using known optical and etch parameters

h) applying corrections to edge segments selected in step f) applying the correction only where it is needed and only in the amount based on the acceptable range of geometry distortion determined in step d) for all devices

i) incorporating said corrections into final corrected photomask features

2. The method of yield improvement of VLSI integrated circuits according to claim 1 in which TCAD simulations are used for extracting nominal device models in step c) of claim 1

3. The method of yield improvement of VLSI integrated circuits according to claim 1 in which TCAD simulations are used for calculating device sensitivities to geometry distortions in step c) of claim 1

4. The method of yield improvement of VLSI integrated circuits according to claim 1 in which TCAD simulations are used exclusively for both extracting nominal device models and calculating device sensitivities to geometry distortions in step c) of claim 1

5. The method of yield improvement of VLSI integrated circuits according to claim 1 further comprising the below steps to be performed after step h) and before step i) of claim 1:

a) simulation of lithographic process as in step g) of claim 1

b) quantifying geometric distortions of the segments identified in step f) of claim 1

6. The method of yield improvement of VLSI integrated circuits according to claim 1 further comprising steps outlined below to be performed after step h) and before step i) of claim 1:

c) simulating of lithographic process as in step g) of claim 1

d) quantifying geometric distortions of the segments identified in step f) of claim 1

e) applying corrections as in step h) of claim 1.

7. The method of yield improvement of VLSI integrated circuits according to claim 6 in which steps c) through e) are repeated in the loop until either geometry distortions of all correction segments meet the minimum requirements determined in step d) of claim 1 or preset number of iterations is exceeded.